

Please type a plus sign (+) inside this box → +

PTO/SB/08A (08-00)

Approved for use through 10/31/2002. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Complete if Known

Application Number	10/747,625
Filing Date	December 30, 2003
First Named Inventor	John P. DEVALE
Group Art Unit	Not yet assigned
Examiner Name	Not yet assigned
Attorney Docket Number	42339-193266

Sheet 1 of 1

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
1	Balasubramanian, R., et al. "Reducing the Complexity of the Register File in Dynamic Superscalar Processors." <i>Proc. of the 34th Int. Symposium on Microarchitecture (MICRO34)</i> , Dec. 2001.	
2	Brekelbaum, N., et al., "Hierarchical Scheduling Windows." <i>Proc. of the 35th Int. Symposium on Microarchitecture (MICRO35)</i> , Nov. 2002.	
3	Cruz, K. et al., "Multiple-banked Register File Architectures." <i>Proc. Of the Int. Symposium on Computer Architecture</i> , Jun. 2000.	
4	Gonzalez, A., et al., "Virtual-physical registers." <i>Proc. of the 4th Int. Symposium on High Performance Computer Architecture</i> , Feb. 1998.	
5	Hinton, G., et al., "The Microarchitecture of the Pentium 4® Processor." <i>Intel Technical Journal</i> , Q1 2001, pp. 1-13.	
6	"Intel® Itanium® Architecture Software Developer's Manual." Intel Corporation 2002.	
7	Jiménez, D. and C. Lin, "Dynamic Branch Prediction with Perceptrons," <i>Proc. of the 7th Int. Symposium on High Performance Computer Architecture (HPCA)</i> , 2001.	
8	Kim, I. and Lipasti, M., "Half-Price Architecture." <i>Proc. of the Intl. Symposium on Computer Architecture</i> , 2003.	
9	Kim, N., and Mudge, T., "Reducing Register Ports Using Delayed Write-Back Queues and Operand Pre-Fetch." <i>International Conference on Supercomputing</i> , 2003.	
10	Kumar, R., "Scalable register file organization for a multiple issue microprocessor." <i>I.E.E. Electronics Letters</i> , Vol. 32, No. 7, 28 March 1996, pp. 634-636.	
11	Park, I., et al. "Reducing Register Ports for Higher Speed and Lower Energy," <i>Proc. of the 35th int. Symposium on Microarchitecture (MICRO35)</i> , Nov. 2002.	
12	Postiff, M., et al., "Integrating Superscalar Processor Components to Implement Register Caching." <i>International Conference on Supercomputing</i> , 2001.	
13	Sezenc, A., et al., "Register Write Specialization Register Read Specialization: A Path to Complexity-Effective Wise-Issue Superscalar Processors." <i>Proceedings of the 35th annual ACM/IEEE international symposium on Microarchitecture</i> , 2002, pp. 1-12.	
14	Shivakumar, P., et al., "An Integrated Cache Timing, Power, and Area Model," <i>WRL Research Report</i> , Feb. 2002.	
15	Tseng, J. and K. Asanovic, "Banked Multiported Register Files for High-Frequency Superscalar Microprocessors." <i>Proc. Of the Intl. Symposium on Computer Architecture</i> , 2003.	
16	Yung, R. and Wilhelm, N., "Caching Processor General Registers." <i>In Proceedings of the International Conference on Circuits Design</i> , 1995, pp. 307-312.	
17	Borch, E., Manne, S., Emer, J., Tune, E., "Loose Loops Sink Chips." <i>The Proceedings of the 8th Int. Symp. on High Performance Computer Architecture</i> , 2002, pp. 1-12.	

Examiner
Signature

Jacob Petrash

Date
Considered

3-20-06

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Unique citation designation number. ² See attached Kinds of U.S. Patent Documents. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

DC2-DOCS1-534951

VL-----